



1. Description

1.1. Project

Project Name	NUCLEO-L476RG-example010
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 6.6.1
Date	07/13/2022

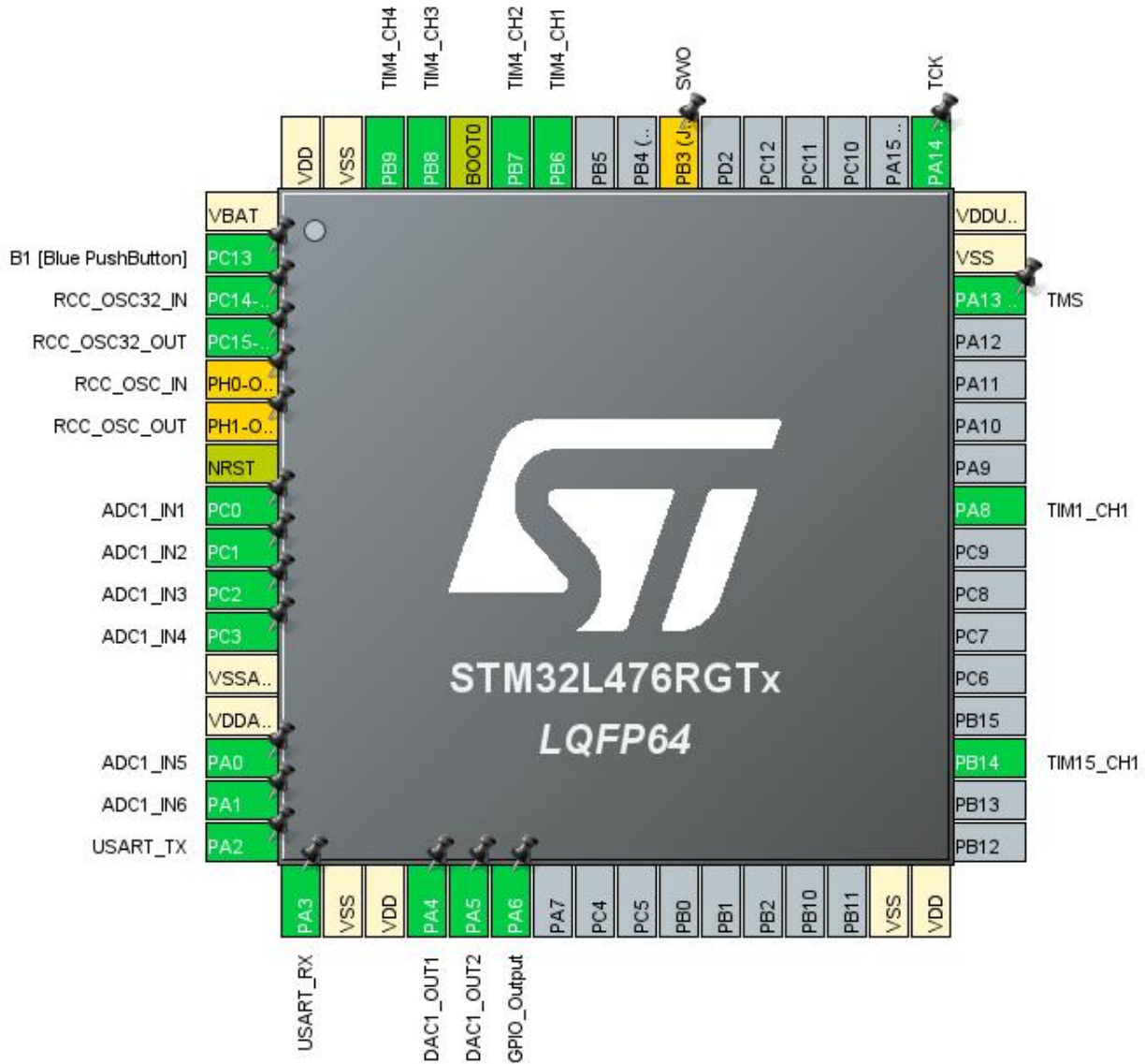
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
---------	---------------

2. Pinout Configuration



3. Pins Configuration

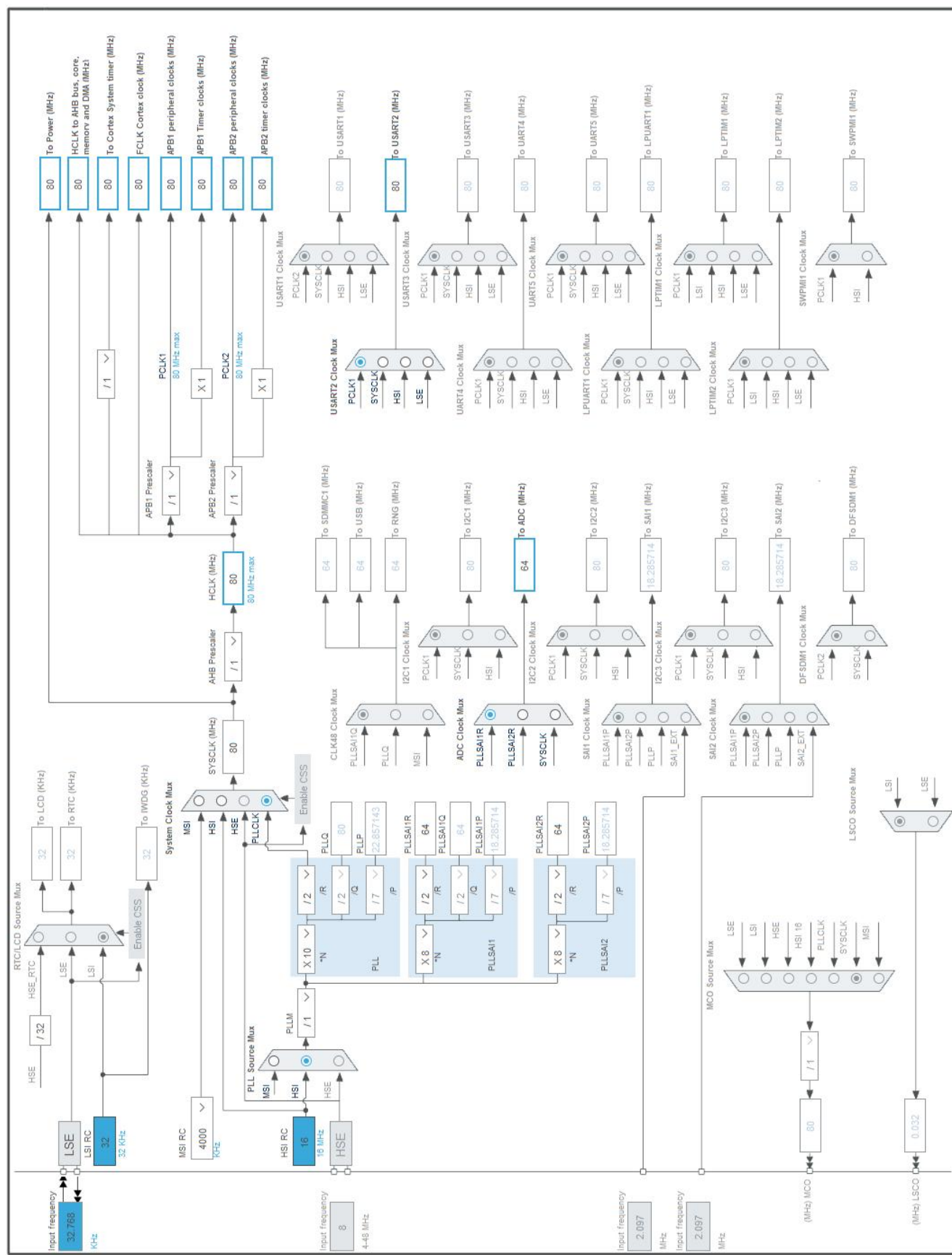
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN1	
9	PC1	I/O	ADC1_IN2	
10	PC2	I/O	ADC1_IN3	
11	PC3	I/O	ADC1_IN4	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	ADC1_IN5	
15	PA1	I/O	ADC1_IN6	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC1_OUT1	
21	PA5	I/O	DAC1_OUT2	
22	PA6 **	I/O	GPIO_Output	
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	TIM15_CH1	
41	PA8	I/O	TIM1_CH1	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	
62	PB9	I/O	TIM4_CH4	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	NUCLEO-L476RG-example010
Project Folder	C:\Users\frank\STM32CubeIDE\workspace_1.10.0\NUCLEO-L476RG-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1
6	MX_DAC1_Init	DAC1
7	MX_TIM1_Init	TIM1
8	MX_TIM3_Init	TIM3
9	MX_TIM4_Init	TIM4
10	MX_TIM15_Init	TIM15

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

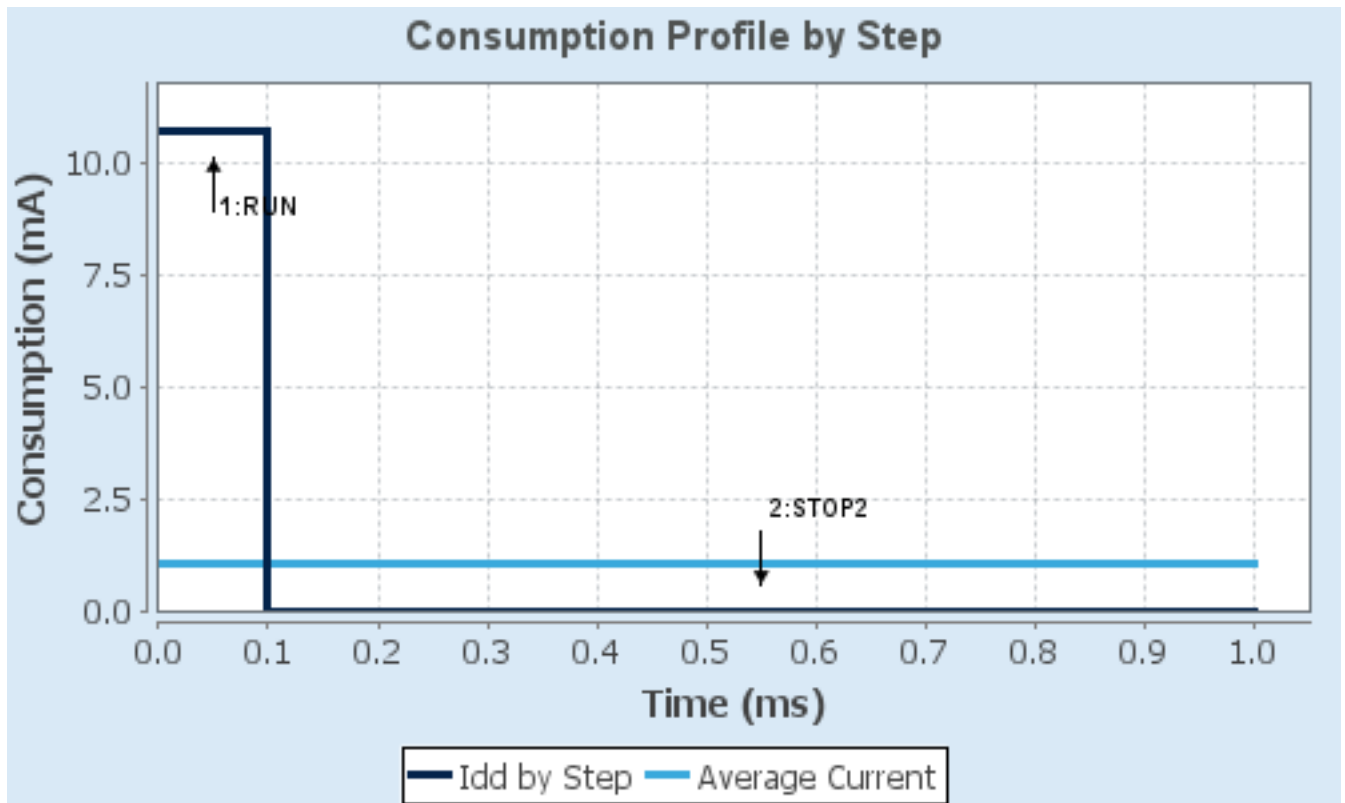
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 μ A
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.56	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

IN6: IN6 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection **End of sequence of conversion ***

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **6 ***

External Trigger Conversion Source **Timer 3 Trigger Out event ***

External Trigger Conversion Edge **Trigger detection on the rising and falling edges ***

Rank 1

Channel Channel 1

Sampling Time 2.5 Cycles

Offset Number No offset

Rank **2 ***

Channel Channel 1

Sampling Time 2.5 Cycles

Offset Number No offset

Rank **3 ***

Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	4 *
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	5 *
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	6 *
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
-----------------------------	---------

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
------------------------------	-------

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
------------------------------	-------

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
------------------------------	-------

7.2. DAC1

OUT1 connected to: only to external pin

OUT2 connected to: only to external pin

7.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.3. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled *
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
-------------------------------	---------------------------------

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture indirect mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	79 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division
Input Filter (4 bits value) 0

Input Capture Channel 2:

Polarity Selection **Falling Edge ***
IC Selection Indirect
Prescaler Division Ratio No division

7.6. TIM3

Clock Source : Internal Clock

Channel1: Output Compare No Output

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) **49 ***
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) **3999 ***
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO **Output Compare (OC1REF) ***

Clear Input:

Clear Input Source Disable

Output Compare No Output Channel 1:

Mode **Toggle on match ***
Pulse (16 bits value) 0
Output compare preload Disable
CH Polarity High

7.7. TIM4

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	39 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	4999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
--------------------	---------

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM15

mode: Clock Source

Channel1: Input Capture direct mode

Channel2: Input Capture indirect mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	79 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Falling Edge *
IC Selection	Indirect
Prescaler Division Ratio	No division

7.9. USART2

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN2	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM15	PB14	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_RX
Single Mapped Signals	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_OUT (PH1)					
	PB3 (JTDO-TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
TIM3 global interrupt	true	9	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
TIM3 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓	ADC1 ✓	TIM1 ✓	USART2 ✓			
GPIO ⚠	DAC1 ✓	TIM3 ✓				
NVIC ✓		TIM4 ✓				
RCC ✓		TIM15 ✓				
SYS ✓						

10. Docs & Resources

Type	Link
------	------